

Abstract of the Disclosure

A clock signal generator varies a frequency of a digital clock over a selected range of frequencies. The generator employs a divider for lowering a frequency of a
5 clock signal. A counter increments synchronously with the signal, and causes a selected sequence of outputs to be generated by a pattern generator. The pattern generator output forms an input to a digitally controllable delay line which receives the lower frequency clock signal. The pattern generator causes the digital delay line to vary a frequency of the lowered frequency clock signal between selected boundaries. The varying frequency
10 clock signal is then raised up again such that a final clock has a varying frequency, and will exhibit less EMI spiking during switching of an associated, synchronous digital data device. The solid state nature of the generator allows for simple fabrication, inexpensive manufacture and ready integration into digital circuitry, such as multifunction integrated circuits.